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Young-Il Kim; Chong-Min Kyung;
Computer Aided Design, 2004. ICCAD-2004. IEEE/AC
Conference on
7-11 Nov. 2004 Page(s):218 - 221
AbstractPlus | Full Text: [PDF\(651 KB\)](#) IEEE CNF
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Maili, A.; Steger, C.; Weib, R.; Quigley, R.; Dalton, D.;
VLSI, 2005. Proceedings. IEEE Computer Society An
on
11-12 May 2005 Page(s):290 - 291
Digital Object Identifier 10.1109/ISVLSI.2005.61
AbstractPlus | Full Text: [PDF\(67 KB\)](#) IEEE CNF
Rights and Permissions
- ☐ **3. An image retrieval system using FPGAs**
Nakano, K.; Takamichi, E.;
Design Automation Conference, 2003. Proceedings o
2003. Asia and South Pacific
21-24 Jan. 2003 Page(s):370 - 373
Digital Object Identifier 10.1109/ASPDAC.2003.11950
AbstractPlus | Full Text: [PDF\(439 KB\)](#) IEEE CNF
Rights and Permissions
- ☒ **4. FPGA based accelerator for functional simulation**
Wageeh, M.N.; Wahba, A.M.; Salem, A.M.; Sheirah, M
Circuits and Systems, 2004. ISCAS '04. Proceedings
International Symposium on
Volume 5, 23-26 May 2004 Page(s):V-317 - V-320 V

[AbstractPlus](#) | [Full Text: PDF\(267 KB\)](#) [IEEE CNF](#)
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- ☐ **5. FPGA hardware devices with single-instruction dr embedded mobile computing platform**
Liu Limin; Salcic, Z.; Li Dong;
[ASIC, 2001. Proceedings. 4th International Conferenc](#)
[23-25 Oct. 2001 Page\(s\):514 - 517](#)
[Digital Object Identifier 10.1109/ICASIC.2001.982613](#)
[AbstractPlus](#) | [Full Text: PDF\(414 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)

- ☒ **6. An FPGA based accelerator for discrete Hartley ar Hadamard transforms**
Amira, A.; Bouridane, A.;
[Circuits and Systems, 2003. MWSCAS '03. Proceedir](#)
[IEEE International Midwest Symposium on](#)
[Volume 2, 27-30 Dec. 2003 Page\(s\):860 - 863 Vol. 2](#)
[Digital Object Identifier 10.1109/MWSCAS.2003.1562](#)
[AbstractPlus](#) | [Full Text: PDF\(2256 KB\)](#) [IEEE CNF](#)
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- ☐ **7. Hardware acceleration of the 3D finite-difference ti method**
Durbano, J.P.; Humphrey, J.R.; Ortiz, F.E.; Curt, P.F.;
Mirotznik, M.S.;
[Antennas and Propagation Society International Sym](#)
[IEEE](#)
[Volume 1, 20-25 June 2004 Page\(s\):77 - 80 Vol.1](#)
[Digital Object Identifier 10.1109/APS.2004.1329557](#)
[AbstractPlus](#) | [Full Text: PDF\(338 KB\)](#) [IEEE CNF](#)
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- ☐ **8. A hardware acceleration simulator for user-defin**
Ying Yu; Hoare, R.R.;
[ASIC, 2003. Proceedings. 5th International Conferenc](#)
[Volume 1, 21-24 Oct. 2003 Page\(s\):199 - 202 Vol.1](#)
[Digital Object Identifier 10.1109/ICASIC.2003.127752](#)
[AbstractPlus](#) | [Full Text: PDF\(338 KB\)](#) [IEEE CNF](#)
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- ☐ **9. Accelerating signal processing algorithms in digit using an FPGA platform**
Lenart, T.; Owall, V.; Gustafsson, M.; Sebesta, M.; Eg
[Field-Programmable Technology \(FPT\), 2003. Procee](#)
[International Conference on](#)
[15-17 Dec. 2003 Page\(s\):387 - 390](#)
[Digital Object Identifier 10.1109/FPT.2003.1275783](#)
[AbstractPlus](#) | [Full Text: PDF\(403 KB\)](#) [IEEE CNF](#)
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- ☐ **10. A fast, inexpensive and scalable hardware accele for functional simulation**
Cadambi, S.; Mulpuri, C.S.; Ashar, P.N.;
[Design Automation Conference, 2002. Proceedings.](#)
[10-14 June 2002 Page\(s\):570 - 575](#)
[Digital Object Identifier 10.1109/DAC.2002.1012690](#)
[AbstractPlus](#) | [Full Text: PDF\(728 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)

- ☐ **11. XCC-a tool for designing parameterizable IP core:**
Mitra, S.;
Signals, Systems, and Computers, 1999. Conference
Thirty-Third Asilomar Conference on
Volume 1, 24-27 Oct. 1999 Page(s):752 - 756 vol.1
Digital Object Identifier 10.1109/ACSSC.1999.832429
AbstractPlus | Full Text: PDF(400 KB) IEEE CNF
Rights and Permissions

- ☐ **12. The Splash 2 software environment**
Arnold, J.M.;
FPGAs for Custom Computing Machines, 1993. Proc
Workshop on
5-7 April 1993 Page(s):88 - 93
Digital Object Identifier 10.1109/FPGA.1993.279475
AbstractPlus | Full Text: PDF(436 KB) IEEE CNF
Rights and Permissions

- ☐ **13. The Splash 2 processor and applications**
Arnold, J.M.; Buell, D.A.; Hoang, D.T.; Pryor, D.V.; Si
M.R.;
Computer Design: VLSI in Computers and Processor
'93. Proceedings., 1993 IEEE International Conference
3-6 Oct. 1993 Page(s):482 - 485
Digital Object Identifier 10.1109/ICCD.1993.393329
AbstractPlus | Full Text: PDF(296 KB) IEEE CNF
Rights and Permissions

- ☒ **14. Hardware/software interface for multi-dimensional
arrays**
Darte, A.; Derrien, S.; Tanguy Risset;
Application-Specific Systems, Architecture Processor
2005. 16th IEEE International Conference on
23-25 July 2005 Page(s):28 - 35
Digital Object Identifier 10.1109/ASAP.2005.38
AbstractPlus | Full Text: PDF(320 KB) IEEE CNF
Rights and Permissions

- ☐ **15. Matlab as a development environment for FPGA c**
Bhatt, T.M.; McCain, D.;
Design Automation Conference, 2005. Proceedings.
13-17 June 2005 Page(s):607 - 610
AbstractPlus | Full Text: PDF(212 KB) IEEE CNF
Rights and Permissions

- ☐ **16. A hardware accelerator IP for EBCOT tier-1 coding
standard**
Tien-Wei Hsieh; Youn-Long Lin;
Embedded Systems for Real-Time Multimedia, 2004.
2004. 2nd Workshop on
2004 Page(s):87 - 90
Digital Object Identifier 10.1109/ESTMED.2004.1359
AbstractPlus | Full Text: PDF(349 KB) IEEE CNF
Rights and Permissions

- ☐ **17. Hardware implementation of genetic algorithm on**
Mostafa, H.E.; Khadrage, A.I.; Hanafi, Y.Y.;
Radio Science Conference, 2004. NRSC 2004. Proc
Twenty-First National

16-18 March 2004 Page(s):C9 - 1-9
 Digital Object Identifier 10.1109/NRSC.2004.1321812
 AbstractPlus | Full Text: [PDF\(453 KB\)](#) IEEE CNF
 Rights and Permissions

- ☐ **18. PARC: a new pyramidal FPGA architecture based processor**
 Rabel, C.E.; Sawan, M.;
Circuits and Systems, 1999. ISCAS '99. Proceedings International Symposium on
 Volume 1, 30 May-2 June 1999 Page(s):470 - 473
 Digital Object Identifier 10.1109/ISCAS.1999.777927
 AbstractPlus | Full Text: [PDF\(272 KB\)](#) IEEE CNF
 Rights and Permissions

- ☐ **19. Automated field-programmable compute acceleration using partial evaluation**
 Qiang Wang; Lewis, D.M.;
FPGAs for Custom Computing Machines, 1997. Proc Annual IEEE Symposium on
 16-18 April 1997 Page(s):145 - 154
 Digital Object Identifier 10.1109/FPGA.1997.624614
 AbstractPlus | Full Text: [PDF\(1028 KB\)](#) IEEE CNF
 Rights and Permissions

- ☐ **20. Use of a soft-core processor in a hardware/software laboratory**
 Chamberlain, R.; Lockwood, J.; Gayen, S.; Hough, R.
Microelectronic Systems Education, 2005. (MSE '05). 2005 IEEE International Conference on
 12-14 June 2005 Page(s):97 - 98
 Digital Object Identifier 10.1109/MSE.2005.63
 AbstractPlus | Full Text: [PDF\(61 KB\)](#) IEEE CNF
 Rights and Permissions

- ☐ **21. Configurable computing architectures for wireless defined radio - a FPGA prototyping experience using design-tool-chains**
 Blaickner, A.; Albl, S.; Scherr, W.;
System-on-Chip, 2004. Proceedings. 2004 International
 16-18 Nov. 2004 Page(s):111 - 116
 Digital Object Identifier 10.1109/ISSOC.2004.141116
 AbstractPlus | Full Text: [PDF\(737 KB\)](#) IEEE CNF
 Rights and Permissions

- ☐ **22. Successful prototyping of a real-time hardware based navigation correlator algorithm**
 Traugott, F.; Andersson, K.; Lofgren, A.; Lindh, L.;
Digital System Design, 2003. Proceedings. Euromicro
 1-6 Sept. 2003 Page(s):334 - 337
 Digital Object Identifier 10.1109/DSD.2003.1231964
 AbstractPlus | Full Text: [PDF\(377 KB\)](#) IEEE CNF
 Rights and Permissions

- ☐ **23. A PLD based encoder interface with accurate position velocity estimation**
 Sisinni, E.; Flammini, A.; Marioli, D.; Taroni, A.;
Industrial Electronics, 2002. ISIE 2002. Proceedings International Symposium on

Volume 2, 8-11 July 2002 Page(s):606 - 611 vol.2
Digital Object Identifier 10.1109/ISIE.2002.1026360
AbstractPlus | Full Text: [PDF\(481 KB\)](#) IEEE CNF
Rights and Permissions

- ☐ **24. Self-sorting radix-2 FFT on FPGAs using parallel distributed arithmetic blocks**
Shaditalab, M.; Bois, G.; Sawan, M.;
FPGAs for Custom Computing Machines, 1998. Proc Symposium on
15-17 April 1998 Page(s):337 - 338
Digital Object Identifier 10.1109/FPGA.1998.707943
AbstractPlus | Full Text: [PDF\(20 KB\)](#) IEEE CNF
Rights and Permissions
- ☐ **25. Virtual prototyping of a digital neural current control**
Dinu, A.; Cirstea, M.N.; McCormick, M.;
Rapid System Prototyping, 1998. Proceedings. 1998 International Workshop on
3-5 June 1998 Page(s):176 - 181
Digital Object Identifier 10.1109/IWRSP.1998.676688
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